SPTCC 2017
Exercises for the wait-free class (Rachid Guerraoui)

Problem 1: from single reader to multiple readers

Consider the transformation (1) from *binary safe* SRSW registers to *binary safe* MRSW register

- Does it work for a *multivalued* register (able to store more than two values)?
- Does it work for *regular* registers (i.e., would it preserve regularity if the base SWSR registers were regular)?
- Does it work for *atomic* registers (i.e., would it preserve atomicity if the base SWSR registers were atomic)?

Problem 2: from binary to M-valued

Consider the transformation (3) from *binary regular* registers to *M-valued regular* Would it preserve *atomicity* if the base binary registers were atomic?

Problem 3: counters

Explain why a *weak counter* can be wait-free implemented from registers, and not a *strong counter*.

Problem 4: FLP

The FLP proof (as presented in the class) relies on two lemmas. Which one makes use of the assumption of having registers as the base objects?